REMARKS/ARGUMENTS

Claims 1-30 are pending in the present application.

This Amendment is in response to the Final Office Action mailed April 20, 2004. In the Final Office Action, the Examiner rejected claims 1, 11, and 21 under 35 U.S.C. §102(a); and claims 2-10, 12-20, 22-30 under 35 U.S.C. §103(a). Reconsideration in light of the remarks made herein is respectfully requested.

Rejection Under 35 U.S.C. § 102 and § 103

1. In the Final Office Action, the Examiner rejected (1) claims 1, 11, and 21 under 35 U.S.C. §102(a) as being anticipated by U.S. Patent No. 6,128,307 issued to Brown ("Brown"), and (2) claims 2-3, 12-13, and 22-23 under 35 U.S.C. §103(a) as being unpatentable over Brown in view of U.S. Patent No. 6,173,385 issued to Tuma et al. ("Tuma") and claims 4-10, 14-20 and 24-30 under 35 U.S.C. §103(a) as being unpatentable over Brown in view of Tuma and further in view of U.S. Patent No. 5,138,696 issued to Nagata ("Nagata"). Applicant respectfully traverses the rejections and contends that the Examiner has not met the burden of establishing a prima facie case of anticipation and obviousness.

Applicant reiterates the arguments set forth in the previously filed Response to the Office Action.

In the Final Office Action, the Examiner made several counter-arguments to Applicant's arguments filed in the previous response. In response to the Examiner's counter-arguments, Applicant addresses these issues in the following.

(i) Block allocation circuit and task coordinator:

The Examiner cited Brown at col. 10, lines 48-57 to support the contention that Brown discloses a block allocation circuit, and Brown at col. 6, lines 62-65 to support the contention that Brown discloses a task coordinator (Final Office Action, page 2, paragraph 4(i)). Applicant respectfully disagrees. First, Applicant notes that by citing Brown at column 10, lines 48-57, and column 6, lines 62-65, the Examiner has changed position from the previous Office Action when the Examiner cited Brown at column 11, lines 59-61 regarding the EXEC routine and column 11, lines 1-3 regarding a timer.

Regarding the block allocation, Brown merely discloses the digital signal processor (DSP) determining a buffer allocation in the memory (Brown, col. 10, lines 52-53). The buffer is used to store the data streams. The DSP communicates to the data flow processor (DFP) that the buffer is available or full (Brown, col. 10, lines 53-57). A buffer allocation is not a block allocation. Furthermore, Brown does not disclose a block allocation circuit. A block allocation circuit allocates blocks of cache memory used by the tasks as recited in claims 1, 11, and 21.

Regarding the task coordinator, Brown merely discloses an interrupt routine handling the interface to the DSP from the DFP and passes control data along to the executive routine (Brown, col. 6, lines 63-65). In contrast, a task coordinator coordinates the tasks in response to a task cycle by the at least one processor as recited in claims 1, 11, and 21. As the examiner may be aware, an interrupt routine is invoked only when there is an interrupt and when the interrupt is enabled. The interrupt routine can only respond to the interrupting device that causes the interrupt. It does not coordinate the tasks in response to a task cycle.

(ii) Product and process claim language:

The Examiner states that if the product is the same as or obvious from a product of the prior art, the claim is unpatentable even the prior product was made by a different process (Final Office Action, page 3, paragraph 4(ii)). In the previous response, Applicant did not simply argue that Brown discloses a program. The main contention was that the EXEC routine does not perform a block allocation function. It does not allocate blocks of cache memory.

(iii) Interrupt routine and Executive routine:

The Examiner cited Brown in column 9, lines 65-68 to column 10, lines 1-8, to support the contention that Brown discloses a block allocation circuit and a task coordinator (Final Office Action, page 3, paragraph 4(iii)). As mentioned earlier, this seems to be inconsistent with the Examiner's contention presented in (i) above. However, assuming the Examiner takes dual positions, this second characterization also fails to support an anticipation rejection. First, storing information on each task is not the same as allocating blocks of cache memory and/or

coordinating tasks in response to a task cycle. The Examiner failed to identify the teaching of a task cycle and coordination of tasks in response to the task cycle. Second, the Examiner failed to identify the allocation of blocks of cache memory taught by Brown.

(iv) Claim interpretation: (Final Office Action, page 3, paragraph 4(iv))

The Examiner failed to interpret the claims consistently with the specification. First, the word "task" used by Brown merely indicates an algorithm (Brown, col. 10, lines 1), not a partitioned program routine viewed as an instruction block with or without a data block, and that can be executed in parallel with other tasks (see specification, for example, page 3, lines 14-25). Second, the task status is not the same as a task table. As shown in Figure 24 of Brown, task status merely indicates whether a task is ready. In contrast, a task table contains the states of active tasks (See, for example, Specification, page 3, line 17). Third, the issues of task coordinator and task cycle have already been discussed earlier.

(v) Search logic and Block information generator:

The Examiner cited Nagata in column 4, lines 10-45 and Figs 23-24 to support the contention that Nagata discloses a search logic circuit (Final Office Action, page 4, paragraph 4(v)). However, nowhere in the cited portions and Figures that such a search logic circuit or its equivalent is disclosed. As discussed in the previous response, Nagata merely discloses a free block retrieve table area that stores free block retrieve flags which represent information about the unused blocks (Nagata, col. 4, lines 43-45). Nagata does not disclose or suggest locating a free block by shifting through a list of busy flags as recited in claims 4, 14, and 24.

The Examiner cited Brown, Figs 23, 24, and 11 to support the contention that Brown discloses a block information generator (Final Office Action, page 4, paragraph 4(v)). However, none of these figures shows a block information generator. The table shown in Figure 11 merely shows a memory mapping of the DSP's address to the generated address. Figure 23 merely shows a flowchart for the EXEC routine task program and a task list. Figure 24 merely shows a flowchart for the EXEC routine task scheduler and the task status. In contrast, a block

information generator generates block information of a free block available for a new task as recited in claims 4, 14, and 24.

(vi) Block starting and ending addresses:

The Examiner states that finding the start and end address of a block of memory for read and write is not different from finding the starting and ending address of a task (Final Office Action, page 4, paragraph 4(vi)). Applicant respectfully disagrees. First, the Examiner takes the phrase out of the context. Within the context of the block information of a free block available for a new task, Tuma does not disclose or suggest the block information. Second, Tuma merely discloses generating address for reading and writing a logical block, not starting and ending addresses associated with a task. The logical block size is selected by the host computer (Tuma, col. 2, lines 35-37), not on a task basis.

(vii) No motivation to combine the references:

The Examiner merely directed Applicant's attention to sections (i) and (ii) without addressing the issue of motivation to combine (Final Office Action, page 5, paragraph 4(vii)). The Examiner also failed to present a convincing line of reasoning as to why a combination of the cited references is an obvious application of a task-based multiprocessor system.

Therefore, Applicant believes that independent claims 1, 11, 21 and their respective dependent claims are distinguishable over the cited prior art references. Accordingly, Applicant respectfully requests the rejection under 35 U.S.C. §102(a) and 35 U.S.C. §103(a) be withdrawn.

Conclusion

Applicant respectfully requests that a timely Notice of Allowance be issued in this case.

Respectfully submitted,

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP

Dated: June 21, 2004 By

Thinh V. Nguyen
Reg. No. 42,034
Tel.: (714) 557-3800 (Pacific Coast)

12400 Wilshire Boulevard, Seventh Floor
Los Angeles, California 90025

CERTIFICATE OF MAILING/TRANSMISSION (37 CFR 1.8A)

I hereby certify that this correspondence is, on the date shown below, being:

MAILING

☐ *deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner for Patents, PO Box 1450, Alexandria, VA 22313-1450.*

Date: 06/21/2004

FACSIMILE

☒ *transmitted by facsimile to the Patent and Trademark Office.*

06/21/2004

Tu Nguyen *Date*